Abstract of the Disclosure:

A test configuration for testing a plurality of integrated circuits, in particular fast semiconductor memory modules located on a wafer, in parallel. The test configuration includes a carrier board for bringing up electrical signal lines belonging to a test system, contact-making needles for producing electrical connections with contact areas on the circuits to be tested, and a plurality of active modules that are arranged on the carrier board. The active modules are each assigned to one of the circuits to be tested in parallel, and are each case inserted into the signal path between the test system and the associated circuit to be tested. In a preferred embodiment, the active modules are arranged at least partly overlapping, based on a direction at right angles to the plane of the carrier board.

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